are "adhered" to the upper surface of the carrier substrate to ensure that it is clear that the chips are not formed or integrated into the upper surface. The marked-up version of the Claim Amendment is show in the Attachment submitted herewith.

Rejection under 35 U.S.C. § 112

Applicant appreciates the Examiner's withdrawal of the rejection of Claim 11.

Rejection under 35 U.S.C. § 103

Claims 1, 4-9 and 12-13 allegedly stand rejected under 35 U.S.C. 103(a) as being unpatentable over Ho (4,254,445) in view of Houston (US 6,362,117 B1) and Ferri (4,326,180). In particular, the Examiner states that:

> "Ho teaches a common carrier, comprising: a carrier substrate **9** having an upper surface wherein the carrier substrate includes a plurality of slots **11** for adhering the plurality of chips. . . However, Ho fails to teach an unprocessed integrateable chip on a carrier substrate. Ferri teaches an unprocessed integrateable chip **20** on a carrier substrate **14** . Houston teaches lithographic alignment tolerances . . Therefore, it would be obvious to one having ordinary skill in the art at the time the invention was made to modify the structure of Ho with lithographic tolerance of Houston and the unprocessed integrateable circuit chip of Ferri to increase frequency".

Claims 1-13

Currently, common carriers are fabricated by placing a plurality of integrated chips on a carrier substrate surface with precision placement tools. As a result, alignment tolerances between the chips are dependent on the placement tools. This type of placement tolerance is inadequate in applications in which alignment of the integrated chips on the carrier substrate is crucial, such as printhead applications. The invention as recited in Claims 1-13 overcomes this alignment problem by providing a common carrier comprising a carrier substrate and a plurality of integrated chips disposed on the surface of the substrate and having an alignment with each other and the substrate within lithographic alignment tolerances.

Ho

Ho describes a "package which comprises a substrate 9 (Fig. 1) upon which is mounted an array of microcircuit chips 10 . . . ", (column 2, lines 63-67). Ho is primarily concerned with the peripheral area 11 about each chip and the fan-out of connection of pads to optimize engineering change and testing connections and, in particular, to provide a packaging scheme where changes can be made with minimal expense, maximum flexibility (column 2, lines 8-14). Ho neither teaches nor suggests any type of alignment between the microcircuit chips 10.

Houston

Houston relates to a technique for forming an integrated circuit "where components of the integrated circuit are very closely spaced, and in some cases by distances which are sublithographic." Houston uses the term "component" to refer to the integrated devices of an integrated circuit. In column 1, lines 49-58 Houston does no teach or suggest the formation of a carrier substrate of integrated chips adhered on the upper surface of a carrier substrate and aligned with each other and the substrate with a lithographic alignment tolerance as recited in Claim 1. Instead, Houston describes fabrication of "components" of an integrated device. In particular, Houston states that "there are limitations on the capability to **fabricate component parts of an integrated circuit** which are very closely spaced." and "there are mechanical considerations which limit the ability to achieve close alignment tolerances between successive **lithographic steps that are involved in the fabrication of an integrated circuit**." (emphasis added). Houston is clearly describing issues involved with the formation of integrated devices in an integrated process not issues relating to the mounting of components on a carrier substrate.

Ferri

Ferri describes a circuit having a semiconductor element 20. The element 20 is a doped semiconductor chip with an alloyed metal dot 30 with gold deposited on its bottom surface. The element is mounted/pre-joined with other circuit components (Fig. 3) and then is immersed into an etchant to further process the semiconductor element. Although Ferri states that the semiconductor element 20 is unprocessed (column 6, line 27), it clearly has been processed prior to mounting. Specifically, element 20 has been 1) doped; 2) has gold deposited on its bottom surface; and 3) has a metal dot 30 deposited on its top surface to form the PN junction (column 4, line 28-30) all prior to mounting. It is clear that what Ferri means by describing semiconductor element 20 as "unprocessed" is that it has not undergone the etching step that is performed once element 20 is joined. Further, Ferri utilizes the term "pre-join" to indicated that the semiconductor element 20 is joined prior to the etching step. Hence, Applicant respectfully submits that semiconductor element 20 has been preprocessed prior to being mounted.

The purpose of Ferri mounting semiconductor element 20 prior to etching element 20 is to minimize handling of the back diode that is created after the etching step. In particular, prior art back diodes are formed by performing the etching step prior to mounting. In this case, the resulting back diode had a fragile neck portion as shown in Fig. 4. Handling the back diode after formation of this thin neck portion was problematic. Hence, Ferri solved this problem

by etching the element 20 to form the fragile neck portion after it has been mounted to minimize problems that occurred when subsequently handling the back diode.

Claims 1-13 are not unpatentable in view of Ho, Houston, and Ferri

As stated above, amended Claim 1 recites, in part, a carrier substrate having an upper surface and a plurality of integrated chips adhered on the upper surface and aligned with each other and the substrate within a lithographic alignment tolerance.

Ho describes an array of processed chips but does not teach any specific alignment between chips or any method of fabrication to suggest a specific alignment tolerance.

Houston describes fabrication of "components" of an integrated device. Houston does not teach or suggest lithographic alignment tolerance of a plurality of integrated chips adhered on the upper surface of a carrier substrate that are aligned with each other and the substrate. Instead, Houston describes lithographic tolerances of components in an integrated circuit.

Ferri teaches a semiconductor element 20 that is partially processed by forming a gold layer on one side and a dot 30 on another side prior to mounting and them processed (i.e., etched) after mounting to avoid handling of the etched semiconductor element. Ferri neither teaches nor suggests forming an array of chips (i.e., elements 20). Moreover, considering the combination of Ferri and Ho, even if an array of elements 20 were formed according to the processing method described by Ferri, (i.e., forming a plurality of semiconductor elements 20 each having a layer of deposited gold and the dot 30 and then mounting and etching the elements), the elements 20 would not be lithographically aligned since dots 30 would be formed prior to mounting and would be aligned between elements 20 according to the mounting tool not according to lithographic alignment tolerances. Hence, the combination of Ho and Ferri teach away from the carrier as recited in Claims 1-13. Ho and Houston are not combinable since they discuss two different technologies resulting in two different products: chips mounted on a substrate (Ho) and devices integrated within a substrate (Houston). Consequently, since neither Ho, Houston, nor Ferri teach or suggest individually or in combination a carrier substrate having an upper surface and a plurality of integrated chips adhered on the upper surface and aligned with each other and the substrate within a lithographic alignment tolerance, Claims 1-13 would not have been unpatentable.

Other Rejections under 35 U.S.C. § 103(a)

Claim 2 allegedly stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Ho, Houston, and Ferri as applied in claim 1 above, and further in view of Yao (6,163,068);

Claim 3 allegedly stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Ho, Houston, and Ferri as applied in claim 1 above, and further in view of Akram (2001/0014488A1);

Claim 10 allegedly stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Ho, Houston, and Ferri as applied in claim 1 and 5-7 above, and further in view of Bayan et al. (6,372,539 B1);

Claim 11 allegedly stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Ho, Houston, and Ferri as applied in claim 1 and 58-9 above, and further in view of Moser et al. (4,797,780).

Since Claims 2, 3, 10, and 11 are all dependent on Claim 1 and since each recited, in part, a carrier substrate having an upper surface and a plurality of integrated chips disposed on the upper surface and aligned with each other and the substrate within a lithographic alignment tolerance, the same argument present above applies to the above alleged rejections of Claims 2, 3, 10 and 11.

Accordingly, Applicants respectfully submit that the rejection under 35 U.S.C. §103(a) have been overcome by these remarks and amendments. This application is now in condition for allowance and such action is earnestly solicited. Withdrawal of all rejections is respectfully requested.

Respectfully submitted,

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ATTACHMENT

1. **(Amended)** A common carrier, comprising:

a carrier substrate having an upper surface; and

a plurality of integrated chips [disposed] adhered on the upper surface and aligned with each other and the substrate with a lithographic alignment tolerance.